ABSTRACT OF THE DISCLOSURE

A semiconductor device having a memory region in which a memory cell array is formed of non-volatile memory devices arranged in a matrix of plurality of rows and columns. Each of the non-volatile memory devices has: a word gate formed above a semiconductor layer with a gate insulating layer interposed; an impurity layer formed in the semiconductor layer to form a source region or a drain region; and sidewall-shaped control gates formed along both side surface of the word gate. Each of the control gates consists of a first control gate and a second control gate adjacent to each other. The first control gate and the second control gate are respectively formed on insulating layers having different thickness.